WHAT IS CLAIMED IS:

1. An apparatus for down-converting an electromagnetic signal, comprising:

a first and second capacitor each having a first and second port;

a first and second switching device each having a first, second, and third port; and

a first and second impedance device each having a first and second port, wherein

the second port of the first capacitor is electrically coupled to the second port of the first switching device and the second port of the first impedance device,

the second port of the second capacitor is electrically coupled to the second port of the second switching device and the second port of the second impedance device, and

the first port of the first switching device is electrically coupled to the first port of the second switching device and the first port of the first and second impedance device, and wherein

a first switching signal is applied to the third port of the first switching device, and

a second switching signal is applied to the third port of the second switching device.

2. The apparatus of claim 1, wherein

the first capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the first switching device is open, and

the second capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the second switching device is open.

3. The apparatus of claim 1, wherein

the first capacitor discharges between six percent to twenty-five percent of the total charge stored therein during a period of time that the first switching device is open, and

the second capacitor discharges between six percent to twenty-five percent of the total charge stored therein during a period of time that the second switching device is open.

4. The apparatus of claim 1, wherein

the first capacitor discharges between ten percent to twenty percent of the total charge stored therein during a period of time that the first switching device is open, and

the second capacitor discharges between ten percent to twenty percent of the total charge stored therein during a period of time that the second switching device is open.

5. The apparatus of claim 1, wherein

the first capacitor discharges between fifteen percent to twenty-five percent of the total charge stored therein during a period of time that the first switching device is open, and

the second capacitor discharges between fifteen percent to twenty-five percent of the total charge stored therein during a period of time that the second switching device is open.

6. The apparatus of claim 1, wherein the first impedance device is an input impedance of a first amplifier and the second impedance device is an input impedance of a second amplifier.

7. The apparatus of claim 1, wherein the first and second switching devices are transistors.

8. The apparatus of claim 1, wherein the first and second switching devices are FETs.

9. The apparatus of claim 1, wherein the first and second switching devices are JFETs.

10. The apparatus of claim 1, wherein the first and second switching devices are MOSFETs.

11. The apparatus of claim 1, wherein the first port of the first switching device, the first port of the second switching device, and the first port of the first and second impedance device are each coupled to an AC ground.

12. An apparatus for down-converting an electromagnetic signal, comprising:

a first and second switching device each having a first, second, and third port;

a first and second capacitor each having a first and second port; and

a first and second impedance device each having a first and second port, wherein

the second port of the first switching device is electrically coupled to the first port of the first capacitor and the first port of the first impedance device,

the second port of the second switching device is electrically coupled to the first port of the second capacitor and the first port of the second impedance device, and

the second port of the first capacitor is electrically coupled to the second port of the second capacitor and the second ports of the first and second impedance devices, and wherein

a first switching signal is applied to the third port of the first switching device, and

a second switching signal is applied to the third port of the second switching device.

13. The apparatus of claim 12, wherein

the first capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the first switching device is open, and

the second capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the second switching device is open.

14. The apparatus of claim 12, wherein

the first capacitor discharges between six percent to twenty-five percent of the total charge stored therein during a period of time that the first switching device is open, and

the second capacitor discharges between six percent to twenty-five percent of the total charge stored therein during a period of time that the second switching device is open.

15. The apparatus of claim 12, wherein

the first capacitor discharges between ten percent to twenty percent of the total charge stored therein during a period of time that the first switching device is open, and

the second capacitor discharges between ten percent to twenty percent of the total charge stored therein during a period of time that the second switching device is open.

16. The apparatus of claim 12, wherein

the first capacitor discharges between fifteen percent to twenty-five percent of the total charge stored therein during a period of time that the first switching device is open, and

the second capacitor discharges between fifteen percent to twenty-five percent of the total charge stored therein during a period of time that the second switching device is open.

17. The apparatus of claim 12, wherein the first impedance device is an input impedance of a first amplifier and the second impedance device is an input impedance of a second amplifier.

18. The apparatus of claim 12, wherein the first and second switching devices are transistors.

19. The apparatus of claim 12, wherein the first and second switching devices are FETs.

20. The apparatus of claim 12, wherein the first and second switching devices are JFETs.

21. The apparatus of claim 12, wherein the first and second switching devices are MOSFETs.

22. The apparatus of claim 12, wherein the second port of the first capacitor, the second port of the second capacitor, and the second port of the first and second impedance device are each electrically coupled to an AC ground.

23. An apparatus for down-converting an electromagnetic signal, comprising:

a first and second capacitor each having a first and second port;

a switching device having a first, second, and third port; and

a first and second impedance device each having a first and second port, wherein

the second port of the first capacitor is electrically coupled to the first port of the switching device and the first port of the first impedance device,

the second port of the second capacitor is electrically coupled to the second port of the switching device and the first port of the second impedance device, and

the second port of the first impedance device is electrically coupled to the second port of the second impedance device, and wherein

a switching signal is applied to the third port of the switching device.

24. The apparatus of claim 23, wherein

the first capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the switching device is open, and

the second capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the switching device is open.

25. The apparatus of claim 23, wherein

the first capacitor discharges between six percent to twenty-five percent of the total charge stored therein during a period of time that the switching device is open, and

the second capacitor discharges between six percent to twenty-five percent of the total charge stored therein during a period of time that the switching device is open.

26. The apparatus of claim 23, wherein

the first capacitor discharges between ten percent to twenty percent of the total charge stored therein during a period of time that the switching device is open, and

the second capacitor discharges between ten percent to twenty percent of the total charge stored therein during a period of time that the switching device is open.

27. The apparatus of claim 23, wherein

the first capacitor discharges between fifteen percent to twenty-five percent of the total charge stored therein during a period of time that the switching device is open, and

the second capacitor discharges between fifteen percent to twenty-five percent of the total charge stored therein during a period of time that the switching device is open.

28. The apparatus of claim 23, wherein the first impedance device is an input impedance of a first amplifier and the second impedance device is an input impedance of a second amplifier.

29. The apparatus of claim 23, wherein the switching device is a transistor.

30. The apparatus of claim 23, wherein the switching device is a FET.

31. The apparatus of claim 23, wherein the switching device is a JFET.

32. The apparatus of claim 23, wherein the switching device is a MOSFET.

33. The apparatus of claim 23, wherein the second port of the first impedance device is electrically coupled to an input port of a first operational amplifier and the second port of the second impedance device is electrically coupled to an input port of a second operational amplifier.

34. An apparatus for down-converting an electromagnetic signal, comprising:

a capacitor having a first and second port;

a switching device having a first, second, and third port; and

an impedance device having a first and second port, wherein

the second port of the capacitor is electrically coupled to the first port of the switching device and the first port of the impedance device, and

the second port of the impedance device is electrically coupled to the second port of the switching device, and wherein

a switching signal is applied to the third port of the switching device.

35. The apparatus of claim 34, wherein

the capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the switching device is open.

36. The apparatus of claim 34, wherein

the capacitor discharges between six percent to twenty-five percent of the total charge stored therein during a period of time that the switching device is open.

37. The apparatus of claim 34, wherein

the capacitor discharges between ten percent to twenty percent of the total charge stored therein during a period of time that the switching device is open.

38. The apparatus of claim 34, wherein

the capacitor discharges between fifteen percent to twenty-five percent of the total charge stored therein during a period of time that the switching device is open.

39. The apparatus of claim 34, wherein the impedance device is an input impedance of an amplifier.

40. The apparatus of claim 34, wherein the switching device is a transistor.

41. The apparatus of claim 34, wherein the switching device is a FET.

42. The apparatus of claim 34, wherein the switching device is a JFET.

43. The apparatus of claim 34, wherein the switching device is a MOSFET.

44. The apparatus of claim 34, wherein the second port of the switching device is electrically coupled to an AC ground.

45. An apparatus for down-converting an electromagnetic signal, comprising:

a capacitor having a first and second port;

a switching device having a first, second, and third port; and

an impedance device having a first and second port, wherein

the first port of the capacitor is electrically coupled to the second port of the switching device and the first port of the impedance device, and

the second port of the impedance device is electrically coupled to the second port of the capacitor, and wherein

a switching signal is applied to the third port of the switching device.

46. The apparatus of claim 45, wherein

the capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the switching device is open.

47. The apparatus of claim 45, wherein

the capacitor discharges between six percent to twenty-five percent of the total charge stored therein during a period of time that the switching device is open.

48. The apparatus of claim 45, wherein

the capacitor discharges between ten percent to twenty percent of the total charge stored therein during a period of time that the switching device is open.

49. The apparatus of claim 45, wherein

the capacitor discharges between fifteen percent to twenty-five percent of the total charge stored therein during a period of time that the switching device is open.

50. The apparatus of claim 45, wherein the impedance device is an input impedance of an amplifier.

51. The apparatus of claim 45, wherein the switching device is a transistor.

52. The apparatus of claim 45, wherein the switching device is a FET.

53. The apparatus of claim 45, wherein the switching device is a JFET.

54. The apparatus of claim 45, wherein the switching device is a MOSFET.

55. The apparatus of claim 45, wherein the second port of the capacitor is electrically coupled to an AC ground.

56. An apparatus for up-converting an electromagnetic signal, comprising:

a first and second amplifier having a first, second and third port;

a first and second switching device having a first, second and third port; and

an impedance device having a first and second port, wherein

the second ports of the first and second amplifiers and the first port of the impedance device are electrically coupled together,

the third port of the first amplifier is electrically coupled to the first port of the first switching device,

the third port of the second amplifier is electrically coupled to the first port of the second switching device, and

the second ports of the first and second switching devices and the second port of the impedance device are electrically coupled together, and wherein

a first switching signal is applied to the third port of the first switching device, and

a second switching signal is applied to the third port of the second switching device.

57. The apparatus of claim 56, further comprising:

a first capacitor having a first and second port, wherein the first port of the first capacitor is electrically coupled to the third port of the first amplifier and the second port of the first capacitor is electrically coupled to a first bias; and

a second capacitor having a first and second port, wherein the first port of the second capacitor is electrically coupled to the third port of the second amplifier and the second port of the second capacitor is electrically coupled to a second bias.

58. The apparatus of claim 57, wherein the first and second bias is an AC ground.

59. The apparatus of claim 56, wherein the first and second switching devices are transistors.

60. The apparatus of claim 56, wherein the first and second switching devices are FETs.

61. The apparatus of claim 56, wherein the first and second switching devices are JFETs.

62. The apparatus of claim 56, wherein the first and second switching devices are MOSFETs.

63. An apparatus for up-converting an electromagnetic signal, comprising:

a first and second amplifier each having a first, second and third port;

a first and second switching device each having a first, second and third port; and

a first, second, and third impedance device each having a first and second port, wherein

the second ports of the first and second amplifiers and the second ports of the first and second switching devices and the first port of the first impedance device are electrically coupled together,

the third port of the first amplifier is electrically coupled to the first port of the second impedance device,

the third port of the second amplifier is electrically coupled to the first port of the third impedance device, and

the first ports of the first and second switching devices and the second ports of the first, second and third impedance devices are electrically coupled together, and wherein

a first switching signal is applied to the third port of the first switching device, and

a second switching signal is applied to the third port of the second switching device.

64. The apparatus of claim 63, further comprising:

a first capacitor having a first and second port, wherein the first port of the first capacitor is electrically coupled to the third port of the first amplifier and the second port of the first capacitor is electrically coupled to a first bias; and

a second capacitor having a first and second port, wherein the first port of the second capacitor is electrically coupled to the third port of the second amplifier and the second port of the second capacitor is electrically coupled to a second bias.

65. The apparatus of claim 64, wherein the first and second bias is an AC ground.

66. The apparatus of claim 63, wherein the first and second switching devices are transistors.

67. The apparatus of claim 63, wherein the first and second switching devices are FETs.

68. The apparatus of claim 63, wherein the first and second switching devices are JFETs.

69. The apparatus of claim 63, wherein the first and second switching devices are MOSFETs.

70. An apparatus for up-converting an electromagnetic signal, comprising:

a first and second amplifier each having a first, second and third port; and

a first, second, third and fourth switching device each having a first, second and third port, wherein

the second ports of the first and second amplifiers are electrically coupled together,

the third port of the first amplifier is electrically coupled to the first ports of the first and second switching devices,

the third port of the second amplifier is electrically coupled to the first ports of the third and fourth switching devices,

the second ports of the first and fourth switching devices are electrically coupled together, and

the second ports of the second and third switching devices are electrically coupled together, and wherein

a first switching signal is applied to the third ports of the first and third switching devices, and

a second switching signal is applied to the third ports of the second and fourth switching devices.

71. The apparatus of claim 70, further comprising:

a first capacitor having a first and second port, wherein the first port of the first capacitor is electrically coupled to the third port of the first amplifier and the second port of the first capacitor is electrically coupled to a first bias; and

a second capacitor having a first and second port, wherein the first port of the second capacitor is electrically coupled to the third port of the second amplifier and the second port of the second capacitor is electrically coupled to a second bias.

72. The apparatus of claim 71, wherein the first and second bias is an AC ground.

73. The apparatus of claim 70, wherein the first, second, third, and fourth switching devices are transistors.

74. The apparatus of claim 70, wherein the first, second, third, and fourth switching devices are FETs.

75. The apparatus of claim 70, wherein the first, second, third, and fourth switching devices are JFETs.

76. The apparatus of claim 70, wherein the first, second, third, and fourth switching devices are MOSFETs.

77. An apparatus for up-converting an electromagnetic signal, comprising:

a first and second amplifier each having a first, second and third port;

a switching device having a first, second and third port;

a first and second capacitor each having a first and second port; and

a first and second impedance device each having a first and second port, wherein

the second port of the first and second amplifier are electrically coupled together,

the third port of the first amplifier is electrically coupled to the first port of the first impedance device,

the third port of the second amplifier is electrically coupled to the first port of the second impedance device,

the first port of the switching device and the second port of the first impedance device and the first port of the first capacitor are electrically coupled together, and

the second port of the switching device and the second port of the second impedance device and the first port of the second capacitor are electrically coupled together, and wherein

a switching signal is applied to the third port of the switching device.

78. The apparatus of claim 77, further comprising:

a third capacitor having a first and second port, wherein the first port of the third capacitor is electrically coupled to the third port of the first amplifier and the second port of the third capacitor is electrically coupled to a first bias; and

a fourth capacitor having a first and second port, wherein the first port of the fourth capacitor is electrically coupled to the third port of the second amplifier and the second port of the fourth capacitor is electrically coupled to a second bias.

79. The apparatus of claim 78, wherein the first and second bias is an AC ground.

80. The apparatus of claim 77, wherein the switching device is a transistor.

81. The apparatus of claim 77, wherein the switching device is a FET.

82. The apparatus of claim 77, wherein the switching device is a JFET.

83. The apparatus of claim 77, wherein the switching device is a MOSFET.

84. A method for down-converting an electromagnetic signal, comprising the steps of:

(1) receiving a RF information signal;

(2) electrically coupling the RF information signal to a capacitor;

(3) controlling a charging and discharging cycle of the capacitor with a switching device electrically coupled to the capacitor, wherein the RF information signal is used to store a charge on the capacitor when the switching device is closed, and wherein the capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the switching device is open; and

(4) performing a plurality of charging and discharging cycles of the capacitor, thereby forming a down-converted information signal.

85. The method of claim 84, wherein the capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the switching device is open.

86. The method of claim 84, wherein the capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the switching device is open.

87. The method of claim 84, further comprising the step of amplifying the down-converted information signal.

88. The method of claim 84, further comprising the step of:

removing a carrier signal from the down-converted information signal.

89. The method of claim 88, wherein the carrier signal is removed by filtering the down-converted signal.

90. The method of claim 88, wherein the carrier signal is removed during amplification of the down-converted signal.